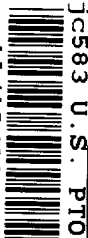


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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)
2. X Specification (Total Pages 46)
(preferred arrangement set forth below)
 - Descriptive Title of the Invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to Microfiche Appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claims
 - Abstract of the Disclosure
3. X Drawings(s) (35 USC 113) (Total Sheets 12)
4. X Oath or Declaration (Total Pages 5)
 - a. X Newly Executed (Original or Copy) (signed)
 - b. Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) (**Note Box 5 below**)
 - i. DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. Microfiche Computer Program (Appendix)

7. ☐ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☒ Assignment Papers (cover sheet & documents(s))
9. ☐ a. 37 CFR 3.73(b) Statement (where there is an assignee)
☐ b. Power of Attorney
10. ☐ English Translation Document (if applicable)
11. ☐ a. Information Disclosure Statement (IDS)/PTO-1449
☐ b. Copies of IDS Citations
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14. ☐ a. Small Entity Statement(s)
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or
☒ Correspondence Address Below
NAME John P. Ward
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
ADDRESS 12400 Wilshire Boulevard
Seventh Floor
CITY Los Angeles STATE California ZIP CODE 90025-1026
Country U.S.A. TELEPHONE (408) 720-8598 FAX (408) 720-9397

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PATENT

UNITED STATES PATENT APPLICATION

FOR

**METHOD AND APPARATUS FOR CALCULATING
INTERCONNECT NOISE DUE TO CROSS CAPACITANCE IN
THE PRESENCE OF LINE RESISTANCE**

INVENTOR:

BEN D. ROBERTS

PREPARED BY:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1026

(408) 720-8598

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METHOD AND APPARATUS FOR CALCULATING INTERCONNECT NOISE DUE TO CROSS CAPACITANCE IN THE PRESENCE OF LINE RESISTANCE

5 FIELD OF INVENTION

The field of the invention relates to electronic circuit simulation. More specifically, the field of invention relates to simplifying the simulation for cross capacitance noise applications.

10 BACKGROUND OF THE INVENTION

Cross Capacitance Noise

Noise is any deviation from a preferred or ideal signal. Applied noise voltages generate undesired voltages or currents (i.e., noise) into a node which affect an otherwise preferred or ideal signal. Multiple noise sources exist within a semiconductor IC (such as AC ripple on the power rails or thermal noise from resistive elements). Another form of noise, referred to as cross capacitance noise (referred to also as cross coupling noise or interconnect noise), occurs where neighboring signal traces are the noise source.

Semiconductor ICs employ metal traces (also referred to as interconnects or interconnect traces) in order to electrically connect transistors. Figure 1a shows a section of two neighboring metal traces 101a, 102a. Typically, the metal traces 101a, 102a are separated and surrounded by dielectric material(s) (not shown).

The combination of a dielectric sandwiched between two conducting traces forms a cross capacitor between the two traces. Thus, simply placing two

interconnect traces 101a, 102a near each other forms a cross capacitor. The interconnect traces 101a, 102a may therefore be modeled as lumped elements 101b, 102b as shown in Figure 1b. That is, a single length of neighboring traces may be viewed as sharing a pair of cross capacitances 108, 109 each having one
5 half the total capacitance between the particular trace length. Each trace 101b, 102b also has an associated series resistance 110, 111. The model of Figure 1b is typical of models used to predict circuit performance.

Capacitances are generally viewed as short circuits for AC signals. Thus a sudden time varying signal on a trace (e.g., time varying signal 112 on trace
10 101b) typically causes noise current 113 to travel from the trace 101b to the neighboring trace 102b. This noise current 113, in turn, causes a voltage perturbation 114 on the neighboring trace 102b. The voltage perturbation 114, when added to any signal on the neighboring trace 102b is typically referred to as cross capacitance noise.

15 As device size continues to shrink (resulting in higher and higher levels of metallization) cross capacitance problems are becoming more severe. The wafer substrate in which devices are embedded is usually grounded so the wafer substrate may be seen as a large ground plane beneath the various pairs of cross-coupled traces. This plane tends to absorb electrical flux lines
20 emanating from the interconnect traces which decrease the cross-capacitance noise. The relationship between the interconnect traces and the grounded

wafer (or to signals on other layers) may be modeled as substrate capacitances
115a,b, 116a,b.

However, the beneficial effect of the grounded wafer is diminished at
higher and higher metallization levels simply because of the increased height of
5 the metal traces above the wafer. Thus, with higher levels of metallization
(necessary to interconnect the expanding number of devices per die), the
industry is experiencing more severe cross capacitance noise problems.

Circuit Modeling

10 Due to the expense associated with manufacturing semiconductor chips
and the competitive nature of the marketplace, it is desirable to have chips
yielding (i.e., the manufacture of working chips suitable for customer shipment)
with the fewest development process runs possible. In order to achieve this,
chip designs are typically simulated by a computing system prior to fabrication.

15 Design defects are discovered during the simulation and the design is fixed
accordingly. The time and expense saved simulating chip designs, as compared
to the alternative approach of making the chip and debugging its design
defects, is considerable.

Given the above described worsening of cross-capacitance noise, it is
20 desirable to simulate its effects. However, as discussed, the noise sources
associated with cross capacitance noise are neighboring signals and trace
geometries. Given the highly complex relationship (in terms of timing, strength,

distances, etc.) between the various signals running over traces, the various geometries between neighboring traces as well as the sheer number of signals and traces, it is extremely cumbersome to completely model these effects.

Specifically, use of SPICE modeling techniques in combination with lumped element models (such as that shown in Figure 1b) requires too much time to simulate. Each trace bend, branch or via creates a new lumped element that must be added to the trace model. A single trace is modeled as a complicated string of lumped elements, each requiring dedicated attention during the simulation. Furthermore, SPICE modeling is an iterative process meaning each of the multiple lumped elements per trace must receive dedicated attention a plurality of times before the simulation is complete. Given the vast number of traces existing within a semiconductor IC, it is simply too inefficient to simulate cross capacitance noise in this manner.

SUMMARY OF THE INVENTION

A method is described that creates a string that models a trace, the string having a collection of lumped elements, where at least one of the lumped elements has a cross capacitor. The method then reduces the string to a pi model where the pi model has a cross capacitor. The method then simulates the application of an applied noise voltage to the cross capacitor.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements, and in which:

- 5 Figure 1A is a depiction of two neighboring traces.
- Figure 1B is a model of the neighboring traces of Figure 1A.
- Figure 2A is a depiction of a trace layout.
- Figure 2B is a string that models the trace of Figure 2A.
- Figure 2C is a single Pi model reduced from the string of Figure 2A.
- 10 Figure 3A is a string that models the trace of Figure 2A.
- Figure 3B is a reduced string created from the string of Figure 3A according to the Elmore influenced method.
- Figure 3C is a simple string created from the second string of Figure 3B.
- Figure 4A shows a section of a simple string.
- 15 Figure 4B shows a reduction of the section of Figure 4A.
- Figure 5A is a string that models the trace of Figure 2A.
- Figure 5B is a reduced string created from the string of Figure 5A according to the O'Brien/Savarino influenced method.
- Figure 6A shows a section of a string having non-zero stub resistance.
- 20 Figure 6B shows a reduction of the section of Figure 6A.
- Figure 7A shows a simulation environment for a single Pi model.
- Figure 7B shows in-phase end of ramp times for applied noise voltages.

Figure 7C shows an example of a piecewise linear noise voltage function.

Figure 7D shows an example of an exponential noise voltage function.

Figure 8A shows source resistance as a function of V_{DS} .

Figure 8B compares a ramp function with the actual rise of a signal
driven by a CMOS driver.

Figure 9A shows proximate conducting traces.

Figure 9B shows a model for the proximate conducting traces of Figure
9A.

Figure 9C shows an approximated model of the model shown in Figure
9B.

Figure 10A shows a string that corresponds to the proximate conducting
trace environment of Figure 9A.

Figure 10B shows the application of an applied noise voltage having an
equivalent ramp time.

Figure 10C shows unique cross capacitances and their associated worst
case applied noise voltages used for calculating the equivalent ramp time
of Figure 10B.

DETAILED DESCRIPTION

A method is described that creates a string that models a trace, the string having a collection of lumped elements, where at least one of the lumped elements has a cross capacitor. The method then reduces the string to a pi model where the pi model has a cross capacitor. The method then simulates the application of an applied noise voltage to the cross capacitor.

These and other embodiments of the present invention may be realized in accordance with the following teachings and it should be evident that various modifications and changes may be made in the following teachings without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense and the invention measured only in terms of the claims.

For example, although the background section alluded mostly to integrated circuits (i.e., silicon chips), the following discussion is perfectly applicable to PC board (also referred to as planar board) technology. Thus, the following discussion is applicable not only to interconnections between transistors on a chip but also to interconnections between silicon chips on a board having a plurality of chips affixed thereto.

Given a trace requiring simulation, a lumped element model of the trace (also referred to as a trace model or string) is created. A lumped element model of a trace is a collection of lumped elements. A lumped element is a model that

corresponds to an important geometrical or electrical feature of the trace (such as a straight length, a bend, a via, a stub, a resistor, a capacitor, an inductor, etc.) Thus, every trace bend, branch or via creates a new lumped element that must be added to the trace model. In order to simulate the effects of cross

5 capacitance noise, each lumped element generally has associated cross capacitances where such cross capacitances exist. Each lumped element is typically a representation of the series resistance, trace to wafer (or other layer) capacitance and cross capacitance associated with that portion of the trace. For example lumped element 101b of Figure 1 has series resistance 110, substrate

10 capacitances 115a,b and cross capacitances 108, 109. Various geometries result in various capacitance and resistance values, thus lumped element values should vary accordingly.

Calculating the specific resistance values follow from Equation 1:

$$R = \frac{\rho L}{A} \quad \text{Equation 1}$$

15 where R is resistance, ρ is the resistivity of the trace material, L is the length of the trace and A is the cross sectional area of the trace (w x t in Figure 1). The cross capacitance for two parallel conducting strips is usually given by:

$$C = \frac{\epsilon tL}{d} \quad \text{Equation 2}$$

where ϵ is the dielectric constant of the dielectric between the traces 101a, 102a

20 and d is the spacing between the traces 101a, 102a. Other additional

relationships may be used as geometries dictate. For example, correction terms may be added to account for field fringing.

A lumped element model of the trace is frequently a complicated string of lumped elements because of all the stubs, vias, etc. Thus a lumped element model of a trace may also be referred to as a string. Such a string 201 is shown in Figure 2b. The string 201 is a model of the circuit trace 202 of Figure 2a. The circuit trace 202 of Figure 2a has three fixed lengths 202a, 203a, 245a, a bend 204a, a via 205a, and stubs 240a, 241a, 242a. Each of these have an associated lumped element model 202b, 203b, 245b, 204b, 205b, 240b, 241b, and 242b as shown in Figure 2b.

Note that stubs 240a,b, 241a,b and 242a,b are typically a load (such as a down stream logic gate input) that the source must drive. Also note the collection of cross capacitances 208. These are the aforementioned cross capacitances between each of the lumped elements and a neighboring trace (not shown in Figure 2A). There is also a collection of substrate capacitances 207. These are aforementioned capacitances between each of the lumped elements and the grounded wafer substrate or lower grounded layers. The substrate capacitances 207 tend to diminish at higher metal layers resulting in greater impedance to ground for cross capacitance noise. As such cross capacitance noise remains on higher metal layer traces rather than shorted to ground.

Note the fixed length lumped element 202b has overlapping capacitance with the bend lumped element 204b. This results from the fact that parallel

capacitances add. That is, fixed length lumped element 202b has its own
capacitance neighboring the bend lumped element 204b. The bend lumped
element 204b has its own capacitance neighboring the fixed length element
202b. This results in neighboring (i.e., parallel) capacitances which may be
5 added together.

As discussed, strings (e.g., string 201) complicate the simulation process.
In order to reduce these complications a simplified model of the string may be
used. For example, the entire string 201 of Figure 2b may be reduced to a single
Pi model 206 (also referred to, among others, as a simple Pi model or Pi model
10 or equivalent Pi) as shown in Figure 2c. Note that the Pi model 206 has a series
resistance 230, a pair of cross capacitances 231a,b and a pair of substrate
capacitances 232a,b. Generally, there is some loss of accuracy when converting
the model from a string (such as string 201) to Pi model 206. However, the loss
of accuracy is acceptable for practical application and the savings in simulation
15 time outweighs the accuracy loss.

A simplification method is used to convert the string 201 to a Pi model
206. A simplification method is any process used to reduce the number of
lumped elements in a string. Two simplification embodiments are described
here: an "Elmore influenced" simplification method and an "O'Brien/Savarino
20 influenced" simplification method. An Elmore influenced simplification
method adds cross capacitance considerations to earlier work done by Elmore
(W.C. Elmore,

"The Transient Response of Damped Linear Networks with Particular Regard to Wide-Band Amplifiers," Jour. Appl. Physics, vol. 19, no. 1, pp. 55-63, January, 1948). An O'Brien/Savarino influenced simplification method adds cross capacitance considerations to earlier work done by O'Brien and Savarino.

- 5 (P.R. O'Brien and T.L. Savarino, "Modeling the Driving-Point Characteristic of Resistive Interconnect for Accurate Delay Estimation," IEEE International Conference on Computer-Aided Design, Digest of Technical Papers pp. 512-515, 1989). Other simplification embodiments may be obtained from basic circuit derivations. Simplification methods as discussed may be implemented in
- 10 software in order to increase design time efficiency.

An Elmore Influenced Simplification Method

- As discussed, various traces may be complicated. For example a trace may be driven by a single driver and then fanned out to multiple receivers (or
- 15 loads). This results in multiple stubs stemming from the main trace to each load. A lumped element model of a trace 301 (also referred to as a string) is shown in Figure 3a. For simplicity, the string 301 is the same string shown back in Figure 2b. Next described is the process of reducing the string 201 of Figure 2b to the pi model 206 of Figure 2c. It should be understood that much of the
- 20 discussion herein, not only for the Elmore influenced simplification method but also for the specification as a whole, employs the use of specific examples. These should not be construed to limit the invention to these specific examples

as they are provided for understanding the broader scope of the invention itself.

Usually, each load has its own unique stub that branches from the main trace and makes contact to the load device. As a result, in one embodiment a preliminary step in the method is to identify the number of different paths existing within the trace. A path is a unique series of lumped elements between a source and a load (or other terminating point). Thus, for traces having fan out (i.e., more than one load) there is typically one path per load. For example, a trace having a single source and a fan out of ten will typically result in ten unique paths. Each path is simplified separately, resulting in a single pi model for each path. Thus, a unique pi model is created for each unique source/load relationship. Some nets may also have more than one driver. In this case a unique path and pi model is created for each source and its relationship with each load. Simulations are typically performed on a per path basis.

In an embodiment, once each path is identified, a single pi model is created for that path. As an example, in Figure 3a, there are three loads 340a, 341a, 342a in string 301, resulting in three paths 370a, 371a, 372a. Analyzing one path at a time, in one approach, stubs (or loads) not associated with the particular path being analyzed are eliminated. This may be accomplished by approximating the stub resistances as having zero resistance. Thus, using path 370a as an example, stub resistances R_1 and R_4 are set to zero. The circuit simulation error introduced by this approximation increases with the length of

the stub. That is, as stub length grows, so too does its resistance. Nevertheless, for trace metallurgy comprising aluminum through SiO₂, the approximation has shown to be acceptable for stubs at least 5mm or less. For other materials such as Copper (Cu) and/or low dielectric constant insulators, the stubs should be greater than 5mm.

Once the stub/load resistances have been approximated as zero, a reduced string 355 (again using the analysis of path 370a as an example) having groups of parallel capacitors (such as parallel capacitor groups 353, 354, 356, 357) will result. A reduced string is a derivative of a string, having less components (e.g. resistors or capacitors) than the string. As parallel capacitance adds, the associated capacitances within each group may be added to form a single capacitor per group. The result is simple string 358 shown in Figure 3c. Simple strings 358 appear as lumped elements of simple trace lengths. That is, simple strings are strings having alternating capacitances and resistances. Again, one simple string exists for each path.

Once the simple string 358 is created, it may be reduced using an Elmore influenced reduction process. For one embodiment, the Elmore influenced reduction process is defined by Figure 4 in combination with Equations 3a-e. Sections (e.g., section 359 of simple string 358 shown back in Figure 3c) having two resistances 401, 402 and six capacitors 403, 404, 405, 406, 407, 408, such as that shown in Figure 4a, may be reduced to one resistor 409 and four

capacitances 410, 411, 412 and 413 as shown in Figure 4b. The equations are given below:

$$R_{\text{new}} = R_1 + R_2 \quad \text{Equation 3a}$$

$$C_{\text{xdnew}} = C_{\text{xd}} + C_{\text{xm}} \left[\frac{R_2}{R_1 + R_2} \right] \quad \text{Equation 3b}$$

$$5 \quad C_{\text{ldnew}} = C_{\text{ld}} + C_{\text{lm}} \left[\frac{R_2}{R_1 + R_2} \right] \quad \text{Equation 3c}$$

$$C_{\text{xrnew}} = C_{\text{xr}} + C_{\text{xm}} \left[\frac{R_1}{R_1 + R_2} \right] \quad \text{Equation 3d}$$

$$C_{\text{lrnew}} = C_{\text{lr}} + C_{\text{lm}} \left[\frac{R_1}{R_1 + R_2} \right] \quad \text{Equation 3e}$$

The reduced model 414 of Figure 4b replaces the original components in the corresponding section 359 of the simple string 358 of Figure 3c. The process is repeated until a simple pi model is left. That is, typically, the process is started at one end (source 380 or load 381 of Figure 3c) of the simple string 358. After each reduction process (which involves new calculations for the new resistor and four capacitors), the simple string is further collapsed toward the other end. Eventually, the simple string is reduced to a pi model.

An O'Brien/Savarino Influenced Simplification Method

Another simplification method is based on the method of O'Brien and Savarino. In one approach, the O'Brien/Savarino influenced method calculates the net admittance at the driver. Similar to the Elmore influenced simplification

method, the O'Brien/Savarino influenced simplification method allows the net to be collapsed to a single Pi equivalent with separate cross capacitors (such as that shown in Figure 2c).

The original O'Brien/Savarino method traverses a net calculating downstream admittance by matching higher moments. Matching moments is equivalent to matching coefficients of S in a Taylor expansion of the downstream admittance. In one embodiment it is applied starting from the receiver load, working toward the driver.

Again, a unique path may be identified for each unique source/load pair (or other terminating point) of a trace. Then each path is reduced to a single pi model. However, as discussed, in this embodiment the O'Brien/Savarino influenced method starts at the load and reduce circuit elements in the direction of the driver. Figure 5 shows a reduction using string 501 as an example. Again, for simplicity, string 201 of Figure 2b is used as string 501.

Also, similarly, path 572a is used as an example.

Whereas Elmore based embodiments may reduce a path to a simple string (such as simple string 358 of Figure 3) by setting branching resistances to zero, O'Brien/Savarino influenced methods tolerate branching resistances and incorporate them into the reduction process. In one approach, parallel capacitances (such as capacitors C_1 , C_2 and C_4 , C_6 in string 501 of Figure 5a) are added in order to form a reduced string (such as reduced string 502 of Figure 5b). Working from load to source, the reduced string 502 is then reduced

further according to an O'Brien/Savarino influenced method. In one embodiment, the O'Brien/Savarino influenced method has two main parts defined by: 1) Figure 4 in combination with Equations 4a-e, 5a-c; and 2) Figure 6 in combination with Equations 6a-e, 7a-c. The equations corresponding to Figure 4 are provided below in Equations 4a-e and 5a-c.

$$R_{new} = \frac{(R_2^2 C_r^3 + 2R_1 R_2 (C_r + C_m) C_r^2 + R_1^2 (C_r + C_m)^3)^2}{(R_2 C_r^2 + R_1 (C_r + C_m)^2)^3} \quad \text{Equation 4a}$$

$$C_{xrnew} = F(C_{xm} + C_{xr}) \quad \text{Equation 4b}$$

$$C_{lmew} = F(C_{lm} + C_{lr}) \quad \text{Equation 4c}$$

$$C_{xdnew} = (1 - F)(C_{xm} + C_{xr}) + C_{xd} \quad \text{Equation 4d}$$

$$C_{ldnew} = (1 - F)(C_{lm} + C_{lr}) + C_{ld} \quad \text{Equation 4e}$$

where:

$$C_r = C_{xr} + C_{lr} \text{ and } C_m = C_{xm} + C_{lm}, \text{ and} \quad \text{Equ. 5a, 5b}$$

$$F = \frac{1}{1 + \frac{R_2^2 C_r^3 C_m}{(R_2 C_r^2 + R_1 (C_r + C_m)^2)^2}} \quad \text{Equation 5c}$$

Furthermore, if a stub or branching load is encountered, the reduction process shown in Figures 6a, 6b is employed where the corresponding equations are as provided below. If there are three or more stubs on a node, then combine them two at a time until a single Pi model remains. Then continue reducing the reduced net toward the driver. Thus an additional aspect of the O'Brien/Savarino influenced method is the use of Figure 6 and Equations 6a-e, 7a-c as just discussed whenever branches occur.

$$R_{\text{new}} = \frac{(R_a^2 C_a^2 + R_b^2 C_b^3)^2}{(R_a C_a^2 + R_b C_b^2)^3} \quad \text{Equation 6a}$$

$$C_{\text{xrnew}} = G(C_{\text{xa}} + C_{\text{xb}}) \quad \text{Equation 6b}$$

$$C_{\text{lmew}} = G(C_{\text{la}} + C_{\text{lb}}) \quad \text{Equation 6c}$$

$$C_{\text{xdnew}} = (1 - G)(C_{\text{xa}} + C_{\text{xb}}) + C_{\text{xc}} \quad \text{Equation 6d}$$

$$C_{\text{ldnew}} = (1 - G)(C_{\text{la}} + C_{\text{lb}}) + C_{\text{lc}} \quad \text{Equation 6e}$$

10 where:

$$C_a = C_{\text{xa}} + C_{\text{la}} \quad \text{and} \quad C_b = C_{\text{xb}} + C_{\text{lb}} \quad \text{Equations 7a,b}$$

$$G = \frac{1}{1 + \frac{C_a C_b (R_a C_a - R_b C_b)^2}{(R_a C_a^2 + R_b C_b^2)^2}} \quad \text{Equation 7c}$$

15 Thus, as the reduction process is continued from load to source for each path (making new calculations along the way), the reduced string (such as reduced string 502 of Figure 5) is ultimately reduced to a single pi model for the unique source/load path that was analyzed.

Cross Capacitance Noise Simulation with the Reduced Pi Models

20 Once the complicated string of a path has been reduced to a simple pi model, noise signals may be introduced at the pi-model's cross-capacitances (e.g., via computer simulation) and their effects on the trace at the source and the load may be studied. Figure 7a shows a single pi model 700 coupled to a source/driver model 703. Simulations may be run with the equivalent circuit in

25 Figure 7a. That is, in one embodiment a resistor (e.g. Ro of Figure 7a) is used to

model the path driver transistor and no additional elements model the load since it was incorporated into the Pi model 700 by the reduction process.

Noise voltages 701a,b are then applied at the cross capacitance tips 702a,b (also referred to as attacking nets). Applied noise sources voltages 701a,b are typically simple voltage ramps (e.g., from 0v to Vcc as shown in Figure 7a) with a rise time duration of T1, T2, respectively. As discussed later, various applied noise types may be applied at the attacking nodes 702a,b. The effects of the applied noise 701a,b are observed at the path's source point 704 and its load point 705. Either of these nodes 704, 705 may be referred to as victim nodes as they are adversely affected by noise introduced from the attacking nodes 702a,b. Applied noise voltages may be worst case signals that could appear on a proximate trace. Worst case signals are those that should induce a large noise voltage on the victim node(s).

For example, the simulator may identify the worst case voltage amplitude (typically Vcc) and shortest ramp time (typically related to device cycle time) that may exist on a neighboring net in actual application. By using these values for the applied noise voltages 701a,b, a worst case scenario may be simulated which provides a high level of confidence that the simulated trace has been properly screened for potential cross capacitance noise problems.

The source model 703 (also referred to as a driver model) is coupled to the source point 704 (also a victim node 704). As discussed in more detail later, the source model 703 may be the driving transistor's source resistance. In the

approach of Figure 7a, the source resistance is grounded because of superposition principles. That is, the effects of the cross capacitance noise are studied individually without specific signals driven by the source transistor onto the path. Thus the voltage source(s) in the simulation embodiment of Figure 7a are only the applied noise source voltages 701a,b. In other embodiments, the driving transistor's signals may be co-simulated with the noise source voltages 701a,b by adding, for example, a current source in parallel with source resistance R_o .

As discussed, the observed cross capacitance noise appearing at the source point 704 and the load point 705 are each found by superpositioning the effects of applied noise voltages 701a,b at each end 704, 705 of the pi model 700. In one approach the noise at the end of the respective ramp times T_1 , T_2 is focused upon. Since cross-capacitance noise originates from sudden voltage changes (such as a rise time voltage swing) the "end-of-ramp" noise is typically the peak noise if the applied noise voltage 701a at the source end 702a has the same amplitude as the applied noise voltage 701b at the load end 702b.

The observed "end of ramp" noise is given by:

$$\frac{V_x}{VCC} = \frac{R_u C_v}{T} \left[1 + \frac{T_A - T_S - 2T_W}{2T_S} e^{-\left(\frac{T_A + T_S}{2T_N}\right)T} - \frac{T_A + T_S - 2T_W}{2T_S} e^{-\left(\frac{T_A - T_S}{2T_N}\right)T} \right] \text{ Equation 8}$$

where, referring to Figure 7,

$$C_{A1} = C_1 + C_{X1} \text{ and } C_{A2} = C_2 + C_{X2} \quad \text{Equations 9a,b}$$

$$T_A = R_o (C_{A1} + C_{A2}) + R_L C_{A2} \quad \text{Equation 9c}$$

$$T_N = R_O R_L C_{A1} C_{A2} \quad \text{Equation 9d}$$

$$T_S = \sqrt{T_A^2 - 4T_N} \quad \text{Equation 9e}$$

and, as provided in Table 1

Table 1

$V_x =$	Noise	R_u	C_v	T	T_w
V_{2A}	At load point 705 from applied noise voltage at the source end 701a	R_O	C_{X1}	T_1	0
V_{2B}	At load point 705 from applied noise voltage at the load end 701b	$R_O + R_L$	C_{X2}	T_2	$\frac{R_O R_L C_{A1}}{(R_O + R_L)}$
V_{1A}	At source point 704 from applied noise voltage at the source end 701a	R_O	C_{X1}	T_1	$R_L C_{A2}$
V_{1B}	At source point 704 from applied noise voltage at the load end 701b	R_O	C_{X2}	T_2	0

Thus, the observed noise voltage at the source point 704 is $V_{1P} = V_{1A} + V_{1B}$

and the observed noise voltage at the load point 705 is $V_{2P} = V_{2A} + V_{2B}$ at the end of the attacking ramp times. These equations correspond to one form of worst case situation (i.e., V_{1P} , V_{2P} are maximum) where the “end of ramp” 707a,b points of the applied noise voltages are in phase. That is, if the ramp ends line up at the same point in time (as shown in Figure 7b), a worst case maximum noise voltage may be observed. The above relationships correspond to such a situation.

The above relationships also correspond to a situation where both ramps reach an amplitude of V_{CC} (i.e., the supply voltage). Thus Equation 8 uses the term V_{CC} . More generically, Equation 8 corresponds to a situation where both applied noise voltage ramps 701a,b have equal amplitude. Thus, in other

situations where Vcc is not the peak voltage but both ramps reach the same amplitude, Equation 8 may still be used provided the Vcc term in Equation 8 is replaced with the appropriate amplitude voltage.

In other cases, the design may involve a worst case situation where applied noise voltage ramps 701a,b have different amplitudes or the two cross capacitances C_{x1} , C_{x2} have different values resulting in different observed noise voltage amplitudes on the victim nodes 704, 705. In such a case, due to the voltage imbalance on the victim nodes 704,705 across the pi model resistor R_L of Figure 7, the peak noise voltages on the victim nodes 704,705 may occur after the ramp end time. The conditions for this imbalance may be expressed as:

$$V_{1P} > V_{2P} \text{ for the load point 705} \quad \text{Equation 10a}$$

$$V_{2P} > \frac{R_o + R_L}{R_o} V_{1P} \text{ for the source point 704} \quad \text{Equation 10b}$$

Either or none of the above conditions can occur (but not both), so one of the noise voltages on a victim node may need correction. The first step is to calculate the time when peak voltage occurs. The following gives the time, after the end of the ramp, where the noise peaks:

$$T_P = \frac{T_N}{T_s} \ln \left[\left(\frac{T_A + T_S}{T_A - T_S} \right) \left(\frac{(T_A - T_S - 2T_X)V_A + 2T_Y V_B}{(T_A + T_S - 2T_X)V_A + 2T_Y V_B} \right) \right] \quad \text{Equation 11}$$

where Equations 9a-e are used together with Table 2 (below) to calculate the corresponding variables for V_{1MAX} and V_{2MAX} .

Table 2

$V_{MAX} =$	Noise	V_A	V_B	T_x	T_y
V_{2max}	At load point 705	V_{2P}	V_{1P}	$R_O C_{A1}$	$R_O C_{A1}$
V_{1max}	At source point 704	V_{1P}	V_{2P}	$(R_O + R_L) C_{A2}$	$R_O C_{A2}$

5 T_p may be substituted into the following expression to find the true peak noise voltage at either the driver (V_{1MAX}) or receiver (V_{2MAX}):

$$V_{max} = \left(\frac{T_A + T_s - 2T_x}{2T_s} V_A + \frac{T_y}{T_s} V_B \right) e^{-\frac{(T_A - T_s)T_p}{2T_N}} - \left(\frac{T_A - T_s - 2T_x}{2T_s} V_A + \frac{T_y}{T_s} V_B \right) e^{-\frac{(T_A + T_s)T_p}{2T_N}}$$

Equation 12

10 Those of ordinary skill will be able to calculate appropriate models for other scenarios such as ramp voltage end times that are not in phase. Also, other embodiments may employ other noise voltage functions besides ramps such as piecewise linear (an example of which is shown in Figure 7c) and
15 exponential (an example of which is shown in Figure 7d).

Once the peak noise voltages are calculated via simulation, the engineer may evaluate whether a cross capacitance noise problem potentially exists on the particular path being simulated. If a potential problem is observed, the

engineer may then, for example, alter the transistor level design or the layout of the trace to properly reduce the cross capacitance noise.

Additional Corrections for CMOS Drivers

5 Note that Figure 7a shows the source model 703 of the driving transistor modeled as a linear resistance, R_o . This is proper for some technologies (such as BiCMOS or Bipolar), however, CMOS drivers or other FET drivers (having noticeably non linear source resistance) may require additional consideration. For example, as shown in Figure 8a, the drain-to-source resistance (i.e., the
10 source resistance) 801a,b of a CMOS driver can gradually increase as V_{ds} increases. This is a non linearity which may lead to an optimistic noise voltage for linear R_o based simulations if the value of R_o employed is too low. To prevent this, in one embodiment, linear R_o based simulations of CMOS driven paths should use values of R_o that correspond to the driver drain current at the
15 maximum noise voltage to be allowed. That is, the employed value of R_o corresponds to a V_{ds} value equal to the maximum noise allowed at the driving node. This approach, however, may lead to a pessimistic noise voltage. Those of ordinary skill can determine an appropriate correction factor if necessary.

 Furthermore, in relation to the applied noise voltages 701a,b of Figure 7,
20 it is assumed that these noise voltages are also driven by a CMOS driver. So far, the discussion has concerned perfect ramps to model these noise voltages 701a,b. As shown in Figure 8b, a ramp 803 is used to approximate a logic level

voltage during its rise time. However, Figure 8b also shows the actual rise time signal 804 that is more typical with CMOS driven nets. The actual slope will normally be measured between two points on the waveform, for example the 20% and 80% points of the attacking driver. While a CMOS output is relatively linear up to the 80% point, after this the ramp drops off quickly and is less effective at inducing noise in the victim. To account for this effect, the applied noise voltage ramp times (T1, T2 of Figure 7) should be multiplied by a factor (1.2 to 1.25 for example) to approximate the noise effect of an actual CMOS waveform.

Multiple Neighboring Traces

So far the discussion has been limited to modeling the effects caused by a single neighboring trace. That is, referring to Figure 1a, if trace 102b is the trace being modeling, only the effects of signals traveling on trace 102a are observed during the modeling analysis of trace102b. However, as shown in Figure 9a, semiconductor IC wiring frequently involves multiple traces 902a,b,c,d within sufficient proximity of each other to cause cross capacitance induced noise.

In order to address multiple noise sources that originate from multiple corresponding proximate traces, the basic lumped element models may be modified, as shown in Figure 9b. Figure 9b shows a lumped element model 903 for a simple length of trace length (e.g., trace length 902a of Figure 9a) having proximate traces (such as traces 902b,c,d of Figure 9a). By comparison, whereas

trace length model 202b of Figure 2b only has one cross capacitance pair 208a, 208b, (resulting in one cross capacitance per node), model 903 of Figure 9b has three cross capacitances (such as cross capacitors 901b,c,d) per node. This follows since each neighboring trace 902b,c,d (referring briefly back to Figure 5 9a) is cross coupled to trace 902a and therefore may act as noise source relative to trace 902a. Thus multiple coupled traces involve more complicated lumped element models having multiple cross capacitances per node. Multiple cross capacitance nodes may be used not only for simple trace lengths (such as that shown in Figure 9b), but are also used for bends, stubs, etc. as well.

10 Multiple cross capacitances per node result in more complicated strings. That is, referring to Figure 2b, if string 201 had three cross capacitances per node the string 201 would have three times the number of cross capacitors 208. The circuit simplification process (to reduce the string to a simple pi model) is therefore further complicated as well. For strings comprising multiple cross 15 capacitances per node, (stemming from multiple trace couplings) the string simplification process requires additional steps as compared to strings having one cross capacitance per node.

The additional step comprises adding the multiple cross capacitances together to form a single cross capacitor (e.g., capacitor 904 as shown in Figure 20 9c) per node as shown. This results in a lumped element model corresponding to a single proximate trace. Once the multiple cross capacitances have been added for each lumped element within a string having multiple cross

capacitances per node, a simple string is eventually created. The reduction process then follows as discussed previously.

The adding of multiple capacitances is an approximation since these capacitances are not truly in parallel. However, an adjustment is made to the applied noise voltages once the single pi model is reached that compensates for this approximation. Specifically, an equivalent noise voltage source that accounts for each of the multiple noise sources (i.e., traces 902b,c,d) is applied to the cross capacitance tips of the pi model.

The adjustment is demonstrated in Figure 10. Again, the structure of Figure 9a serves as the basis for this example. Figure 10a shows a string (i.e., the lumped element model of the trace before any reductions are made) having unique cross capacitances at the source end of the string. Referring to Figure 10b, the applied noise voltage at the source, used with the simple pi model (once its obtained after reduction of the string), has an equivalent ramp time T_{eq} .

Referring to Figure 9c, T_{eq} is obtained from the worst case signal from each of the neighboring traces is. Each signal may have its own unique ramp time (such as ramp times T_1 , T_2 and T_3). The individual cross capacitance values at the source end of the string are then used to calculate the equivalent applied noise voltage ramp time (i.e., T_{eq} of Figure 3b) according to Equation 13, below. Note that these cross capacitance values have already been added together and

incorporated in the single pi model 1005 of the path. However, for purposes of adjusting the applied noise voltage ramp time, their independence is utilized.

$$T_{eq} = \frac{C_{X1} + C_{X2} + C_{X3} + \dots}{\frac{C_{X1}}{T_1} + \frac{C_{X2}}{T_2} + \frac{C_{X3}}{T_3} + \dots} \quad \text{Equation 13}$$

The same analysis may be used at the load end as well. That is, the individual cross capacitance values appearing at the load end of the string are used to generate an effective applied noise voltage ramp time. It is assumed that the attacking ramps all coincide at the same peak ramp time to produce worst case noise. Also, note that Equation 13 is general. That is, Equation 13 applies to situations having more or less than three cross capacitances per node as seen in Figure 10.

Noise Waveform Generation

The single pi model approach may also be used to generate noise waveforms generated at the driver and load. That is, so far only noise peak values have been discussed in order to identify the worst case noise peak. However, in other instances it may be useful to know, approximately, the overall appearance of the noise waveform. This is accomplished by incrementing the overall applied voltage ramp 1101 into incremental voltage valves 1103a,b,c,...n having associated times 1104a,b,c,...n. By using the aforementioned analyses within the pi model 1102, a corresponding

incremental noise voltage 1105a,b,c,...n is produced for each incremental time 1104a,b,c,...n. The collection of noise voltages 1105a,b,c,...n may be plotted against their corresponding times 1104a,b,c,...n to produce the overall noise voltage waveform 1106. For each noise voltage waveform 1106, the

- 5 incremented noise sources may include both the source noise voltage and the load noise voltage or either of these alone depending on the specific purpose of the waveform study.

Design Tool Environment

- 10 The aforementioned methods may be executed within a number of different design tool environments. Design tools are computer programs used to implement a circuit design into hardware. For example, the simulations of the pi model response to the applied noise voltages may be run on SPICE based simulators (such as PSpice for personal computing systems or HSpice for
- 15 workstations). Simulations are computer based executions of circuit models in order to model circuit operation. For SPICE based simulations, a spice model of the pi model and the applied noise voltages may be created. However, the simulations may also be performed on other types of simulators such as proprietary/in-house simulation environments.

- 20 The trace model (i.e., string) may be obtained or derived from the netlist information contained within the layout design tool. Various commercial layout tools (such as CELL3™ OR IC Craftsmen™ by CADENCE™ or other

tools by MENTOR™) as well as proprietary tools exist. Software that executes the reduction processes may be written to help port the trace model information (from the layout netlist) to the pi model (for use in the simulator). This is true in environments where simulation is performed on a separate tool from the layout as well as in tool environments where layout and simulation is integrated.

Design tools are typically implemented with machine readable media. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.

CLAIMS

What is claimed is:

1 1. A machine-readable medium having stored thereon instructions, which
2 when executed by one or more processors, cause said processors to perform the
3 following:

4 a) create a string that models a trace, said string having a collection of
5 lumped elements, at least one of said lumped elements having a cross
6 capacitor;

7 b) reduce said string to a pi model, said pi model having a cross
8 capacitor; and

9 c) simulate the application of an applied noise voltage to said cross
10 capacitor.

1 2. The machine-readable medium of claim 1 wherein said reduce said string to
2 a pi model further comprises reducing the number of capacitors and resistors in
3 said string.

1 3. The machine-readable medium of claim 2 wherein said reducing said string
2 to a pi model further comprises reducing six capacitors and two resistors in said
3 string to four capacitors and one resistor.

1 4. The machine-readable medium of claim 3 wherein said reduction of six
2 resistors and four capacitors is performed according to an Elmore influenced
3 reduction method.

1 5. The machine-readable medium of claim 3 wherein said reduction of resistors
2 and capacitors is performed according to an O'Brien/Savarino influenced
3 reduction method.

1 6. The machine-readable medium of claim 1 wherein said string further
2 comprises a number of paths, said reduction of said string to a pi model
3 performed for one of said paths.

1 7. The machine-readable medium of claim 1 wherein said application of a noise
2 voltage further comprises applying a voltage ramp as said applied noise
3 voltage.

1 8. The machine-readable medium of claim 7 wherein the ramp time of said
2 voltage ramp is multiplied by a factor to correct for the characteristics of an
3 actual driving transistor.

1 9. The machine-readable medium of claim 1 wherein said instructions are such
2 that said reduce said string to a pi model may be performed on a first apparatus

3 and said create a string that models a trace may be performed on a second
4 apparatus.

1 10. The machine-readable medium of claim 1 further comprising instructions
2 that add a resistor to said pi model as a linear source model.

1 11. The machine-readable medium of claim 1 further comprising instructions
2 that allow a user to observe a noise voltage waveform on a victim node of said
3 pi model.

1 12. The machine-readable medium of claim 1 further comprising instructions
2 that calculate the peak noise voltage on a victim node of said pi model caused
3 by said applied noise voltage.

1 13. The machine-readable medium of claim 1 further comprising instructions
2 that apply a second applied noise voltage to a second cross capacitor of said pi
3 model.

1 14. The machine-readable medium of claim 13 wherein said applied noise
2 voltage and said second applied noise voltage are voltage ramps having their
3 end or ramp times in phase.

1 15. The machine-readable medium of claim 13 further comprising instructions
2 that calculate the peak noise caused by said applied noise voltage and said
3 second applied noise voltage at a source point of said pi model.

1 16. The machine-readable medium of claim 13 further comprising instructions
2 that calculate the peak noise caused by said applied noise voltage and said
3 second applied noise voltage at a load point of said pi model.

1 17. The machine-readable medium of claim 1 wherein said reduce said string to
2 a pi model further comprises reducing said string to a reduced string then
3 reducing said reduced string to a simple string having resistors in series and
4 capacitors in parallel, said capacitors separated by one of said resistances, then
5 reducing said simple string to a pi-model.

1 18. A machine-readable medium having stored thereon instructions, which
2 when executed by one or more processors, cause said set of processors to
3 perform the following:

4 a) create a string that models a trace, said string having a collection of
5 lumped elements, at least one of said lumped elements having a
6 plurality of cross capacitors on a node, each of said cross capacitors
7 corresponding to a different proximate trace;

8 b) add said plurality of cross capacitors together to form a reduced
9 string;

10 c) reduce said reduced string to a pi model, said pi model having a
11 cross capacitor; and

12 d) simulate the application of an applied noise voltage to said cross
13 capacitor.

1 19. The machine-readable medium of claim 18 wherein said reduce said
2 reduced string to a pi model further comprises reducing the number of
3 capacitors and resistors in said reduced string.

1 20. The machine-readable medium of claim 19 wherein said reduce said
2 reduced string to a pi model further comprises reducing six capacitors and two
3 resistors in said string to four capacitors and one resistor.

1 21. The machine-readable medium of claim 20 wherein said reduction of six
2 resistors and four capacitors is performed according to an Elmore influenced
3 reduction method.

1 22. The machine-readable medium of claim 20 wherein said reduction of
2 resistors and capacitors is performed according to an O'Brien/Savarino
3 influenced reduction method.

1 23. The machine-readable medium of claim 18 wherein said string further
2 comprises a number of paths, said reduction of said string to a pi model
3 performed for one of said paths.

1 24. The machine-readable medium of claim 18 wherein said apply a noise
2 voltage further comprises applying a voltage ramp as said applied noise
3 voltage.

1 25. The machine-readable medium of claim 24 wherein said voltage ramp
2 further comprises an equivalent ramp time that approximates the worst case
3 noise caused by said plurality of proximate traces.

1 26. The machine-readable medium of claim 18 wherein said instructions are
2 such that said reduce said reduced string to a pi model may be performed on a
3 first apparatus and said create a string that models a trace may be performed on
4 a second apparatus.

1 27. The machine-readable medium of claim 18 wherein said reduce said
2 reduced string to a pi model further comprises reducing said reduced string to
3 a simple string then reducing said simple string to a pi-model.

- 1 28. An apparatus, comprising:
2 a computer having a design tool configured to:
3 a) recognize a string that models a trace, said string having a
4 collection of lumped elements, at least one of said lumped
5 elements having a cross capacitor;
6 b) reduce said string to a pi model, said pi model having a cross
7 capacitor; and
8 c) simulate the application of an applied noise voltage to said
9 cross capacitor.
- 1 29. A machine-readable medium having stored thereon instructions which
2 when executed by one or more processors cause said processors to perform
3 the following:
4 calculate a plurality of discrete samples from an overall applied
5 noise voltage waveform and simulate the application of each of said
6 plurality of discrete samples to a cross capacitor, said cross capacitor
7 associated with a pi model, said pi model reduced from a string.
- 1 30. The machine-readable medium of claim 29 further comprising instructions
2 that assemble a plurality of observed noise voltages from the simulation of
3 the application of each of said discrete samples.

1 31. The machine-readable medium of claim 30 further comprising instructions
2 that display an overall observed noise voltage waveform produced from
3 said plurality of observed noise voltages.

1 32. The machine-readable medium of claim 29 wherein said overall applied
2 noise voltage waveform is a ramp.

1 33. A method, comprising:

- 2 a) create a string that models a trace, said string having a collection of
3 lumped elements, at least one of said lumped elements having a cross
4 capacitor;
5 b) reduce said string to a pi model, said pi model having a cross
6 capacitor; and
7 c) simulate the application of an applied noise voltage to said cross
8 capacitor.

1 34. The method of claim 33 wherein said reduce said string to a pi model
2 further comprises reducing the number of capacitors and resistors in said
3 string.

1 35. The method of claim 34 wherein said reducing said string to a pi model
2 further comprises reducing six capacitors and two resistors in said string to four
3 capacitors and one resistor.

1 36. The method of claim 35 wherein said reduction of six resistors and four
2 capacitors is performed according to an Elmore influenced reduction method.

1 37. The method of claim 35 wherein said reduction of resistors and capacitors is
2 performed according to an O'Brien/Savarino influenced reduction method.

1 38 The method of claim 33 wherein said string further comprises a number
2 of paths, said reduction of said string to a pi model performed for one of
3 said paths.

1 39. The method of claim 33 wherein said application of a noise voltage further
2 comprises applying a voltage ramp as said applied noise voltage.

1 40. The method of claim 39 wherein the ramp time of said voltage ramp is
2 multiplied by a factor to correct for the characteristics of an actual driving
3 transistor.

1 41 The method of claim 33 wherein said reduce said string to a pi model is
2 performed on a first apparatus and said create a string that models a trace is
3 performed on a second apparatus.

1 42. The method of claim 33 further comprising add a resistor to said pi model
2 as a linear source model.

1 43 The method of claim 33 further comprising observe noise voltage on a
2 victim node of said pi model.

1 44. The method of claim 33 further comprising calculate the peak noise voltage
2 on a victim node of said pi model caused by said applied noise voltage.

1 45. The method of claim 33 further comprising apply a second applied noise
2 voltage to a second cross capacitor of said pi model.

1 46. The method of claim 45 wherein said applied noise voltage and said second
2 applied noise voltage are voltage ramps having their end or ramp times in
3 phase.

1 47. The method of claim 45 further comprising calculate the peak noise caused
2 by said applied noise voltage and said second applied noise voltage at a source
3 point of said pi model.

1 48. The method of claim 45 further comprising calculate the peak noise caused
2 by said applied noise voltage and said second applied noise voltage at a load
3 point of said pi model.

1 49. The method of claim 33 wherein said reduce said string to a pi model
2 further comprises reducing said string to a reduced string then reducing said
3 reduced string to a simple string having resistors and capacitors in parallel, said
4 capacitors separated by one of said resistors then reducing said simple string to
5 a pi-model.

1 50. A method, comprising:

- 2 a) create a string that models a trace, said string having a collection of
3 lumped elements, at least one of said lumped elements having a
4 plurality of cross capacitors on a node, each of said cross capacitors
5 corresponding to a different proximate trace;
- 6 b) add said plurality of cross capacitors together to form a reduced string;
- 7 c) reduce said reduced string to a pi model, said pi model having a cross
8 capacitor; and

9 d) simulate the application of an applied noise voltage to said cross
10 capacitor.

1 51. The method of claim 50 wherein said reduce said reduced string to a pi
2 model further comprises reducing the number of capacitors and resistors in
3 said reduced string.

1 52. The method of claim 51 wherein said reduce said reduced string to a pi
2 model further comprises reducing six capacitors and two resistors in said string
3 to four capacitors and one resistor.

1 53. The method of claim 52 wherein said reduction of six resistors and four
2 capacitors is performed according to an Elmore influenced reduction method.

1 54. The method of claim 52 wherein said reduction of resistors and capacitors is
2 performed according to an O'Brien/Savarino influenced reduction method.

1 55. The machine-readable medium of claim 50 wherein said string further
2 comprises a number of paths, said reduction of said string to a pi model
3 performed for one of said paths.

1 56. The method of claim 50 wherein said apply a noise voltage further
2 comprises applying a voltage ramp as said applied noise voltage.

1 57. The method of claim 56 wherein said voltage ramp further comprises an
2 equivalent ramp time that approximates the worst case noise caused by said
3 plurality of proximate traces.

1 58. The method of claim 50 wherein said reduce said reduced string to a pi
2 model is performed on a first apparatus and said create a string that models a
3 trace is performed on a second apparatus.

1 59. The method of claim 50 wherein said reduce said reduced string to a pi
2 model further comprises reducing said reduced string to a simple string then
3 reducing said simple string to a pi-model.

1 60. A method, comprising:
2 calculate a plurality of discrete samples from an overall applied
3 noise voltage waveform and simulate the application of each of said
4 plurality of discrete samples to a cross capacitor, said cross capacitor
5 associated with a pi model, said pi model reduced from a string.

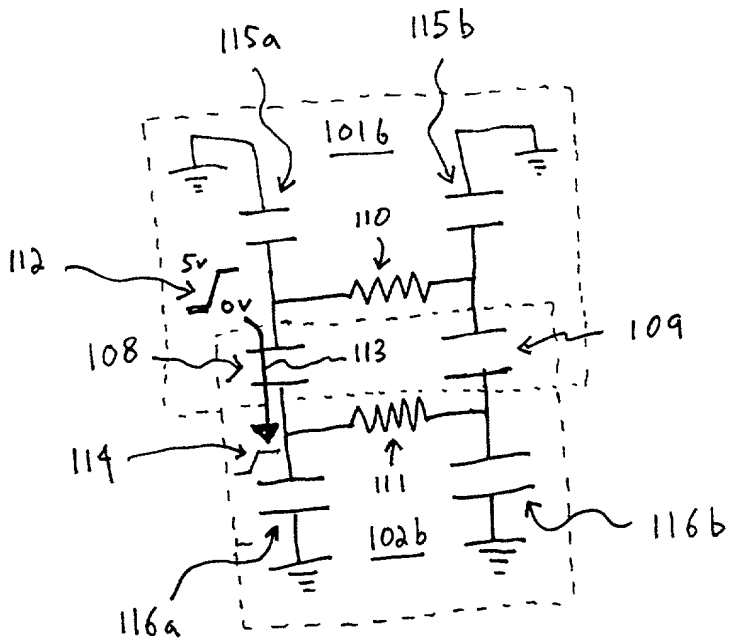
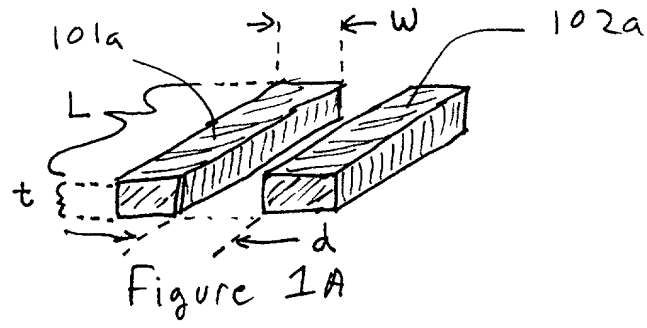
1 61. The method of claim 60 further comprising assemble a plurality of
2 observed noise voltages from the simulation of the application of each of said
3 discrete samples.

1 62. The method of claim 61 further comprising display an overall observed
2 noise voltage waveform produced from said plurality of observed noise
3 voltages.

1 63. The method of claim 60 wherein said overall applied noise voltage
2 waveform is a ramp

ABSTRACT

A method that creates a string that models a trace, the string having a collection of lumped elements, where at least one of the lumped elements has a cross capacitor. The method reduces the string to a pi model where the pi model has a cross capacitor. The method simulates the application of an applied noise voltage to the cross capacitor.



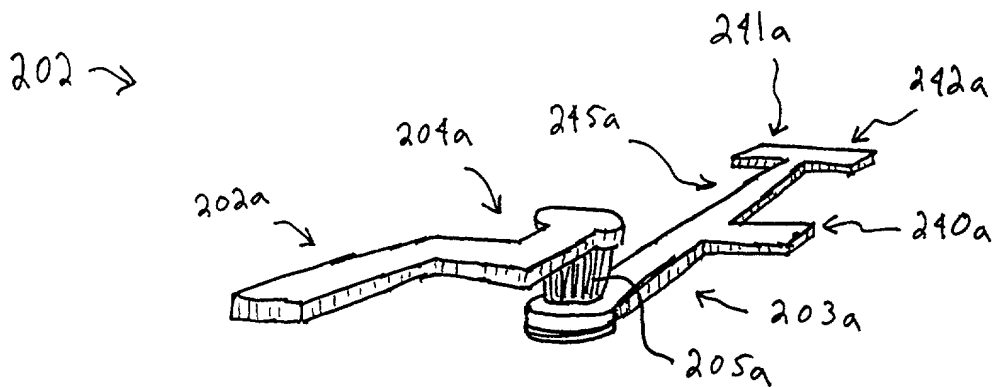


FIGURE 2A

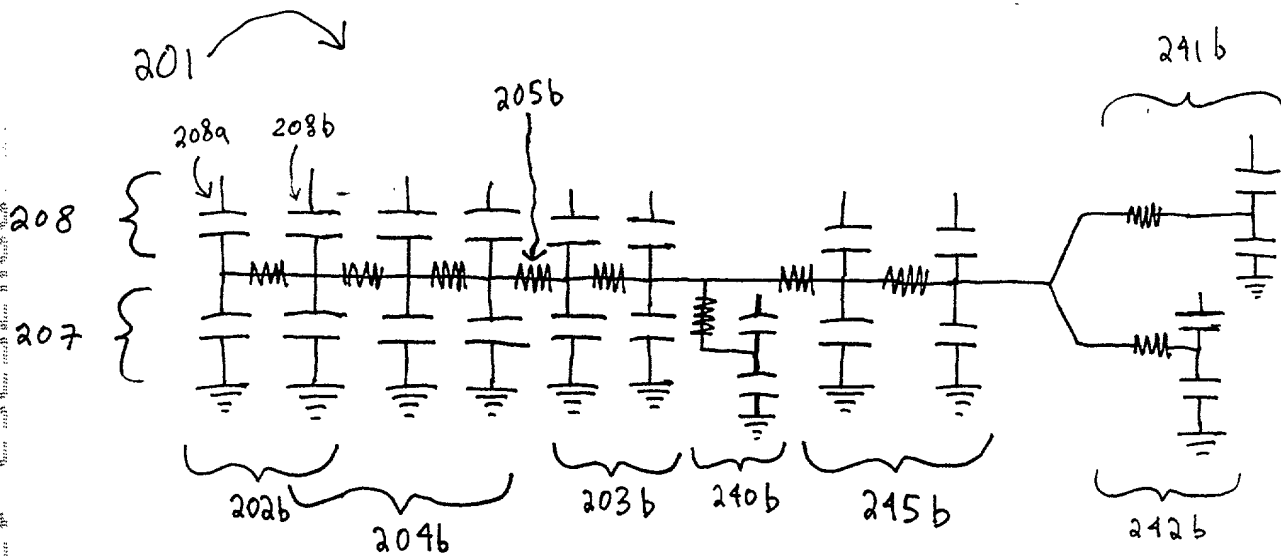


FIGURE 2B

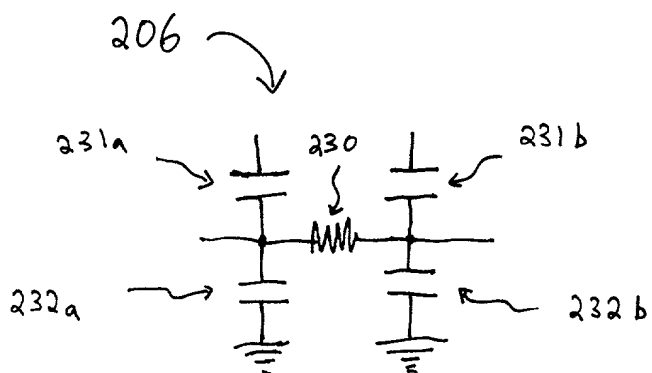
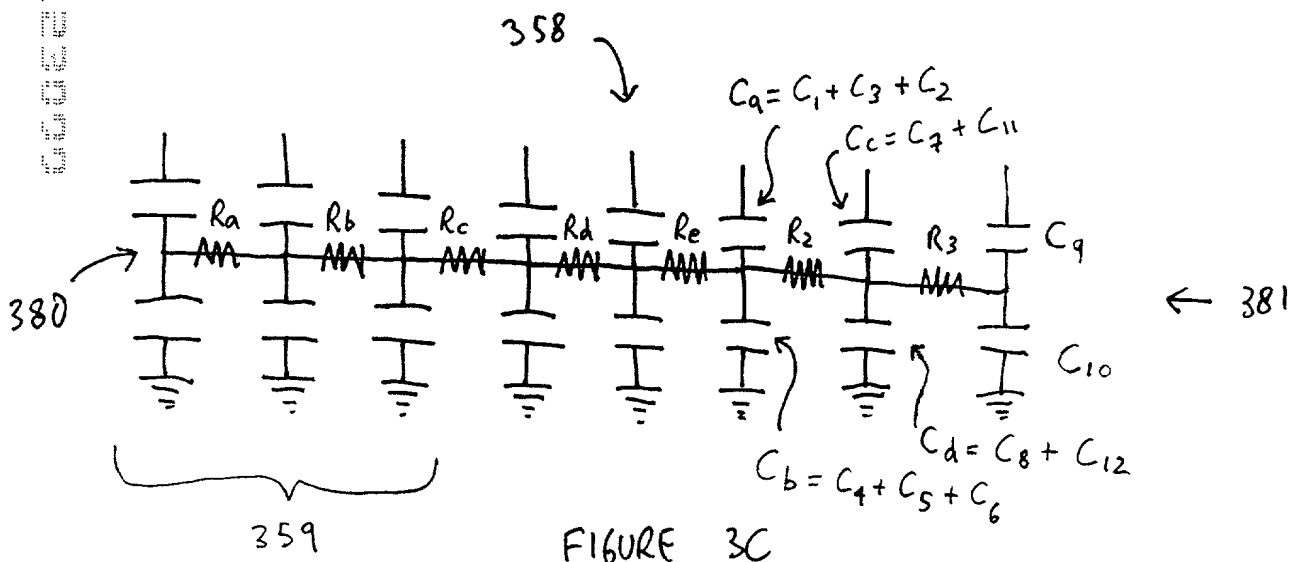
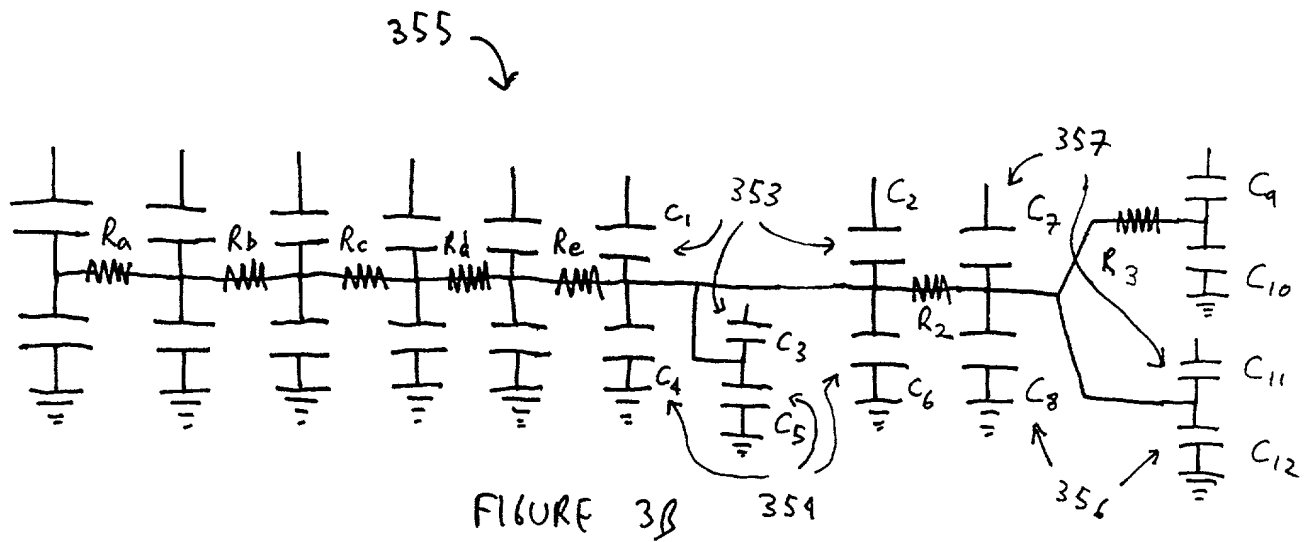
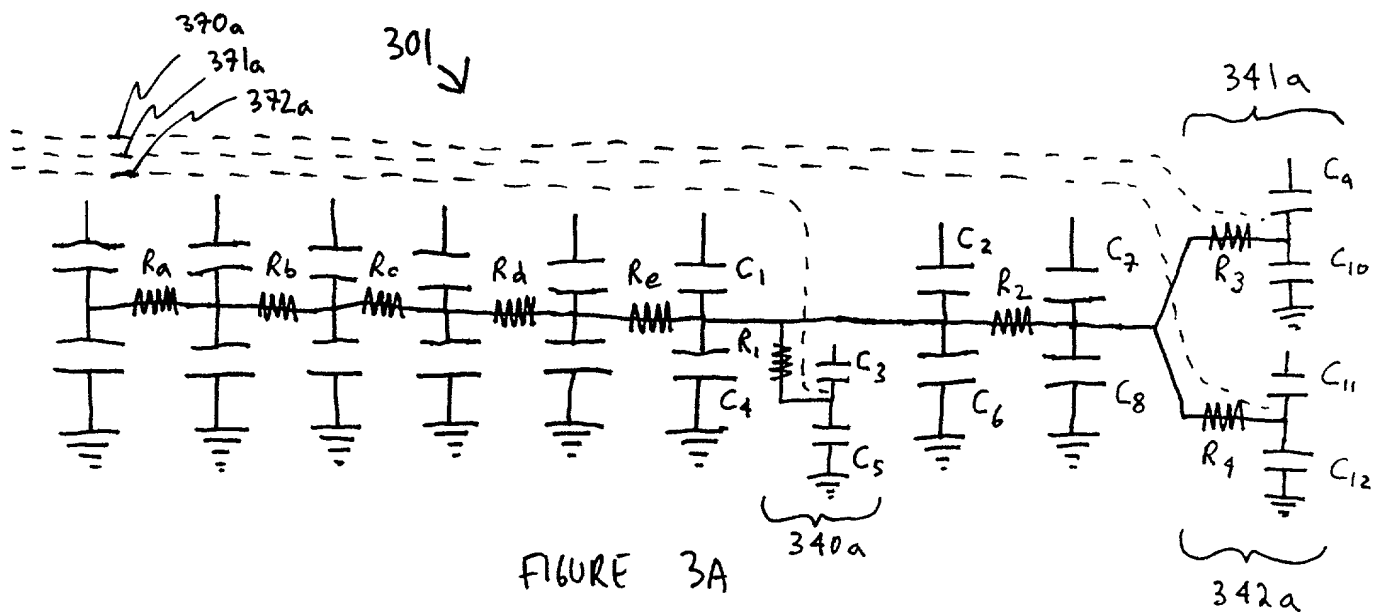


FIGURE 2C



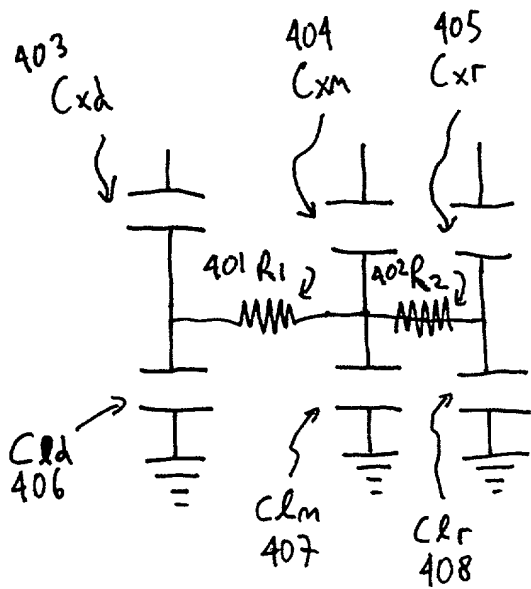


FIGURE 4A

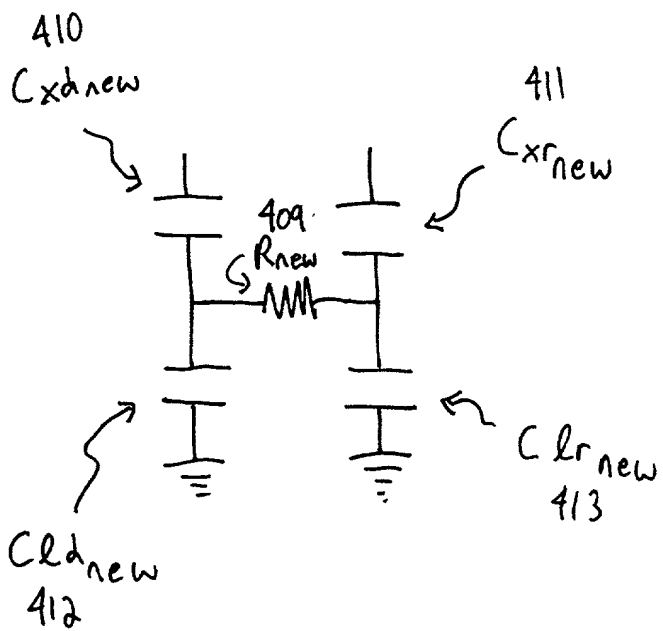


FIGURE 4B

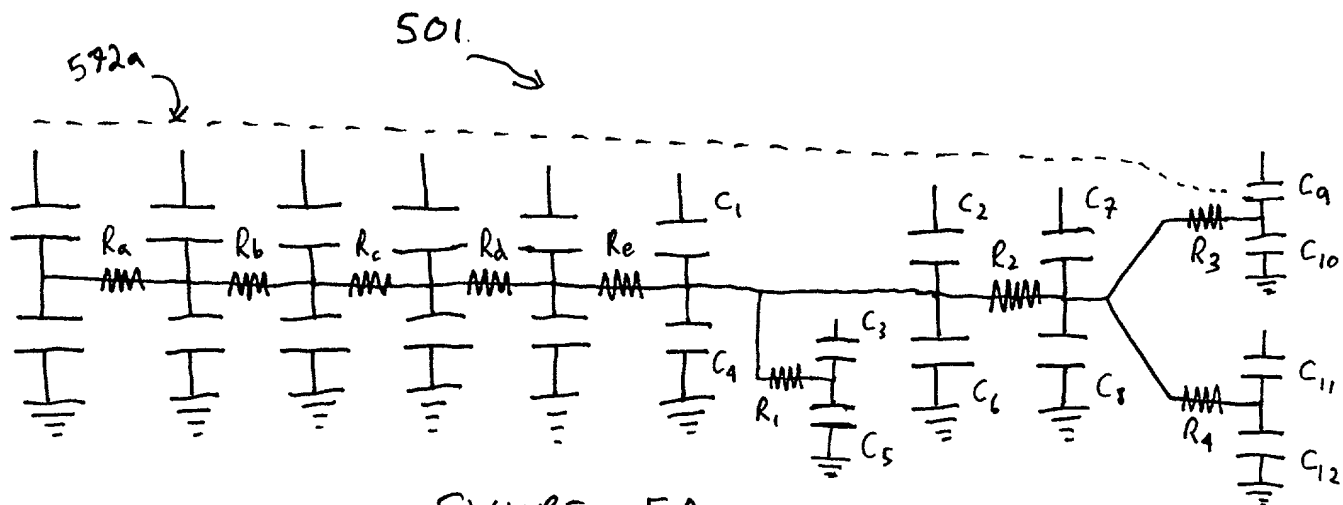


FIGURE 5A

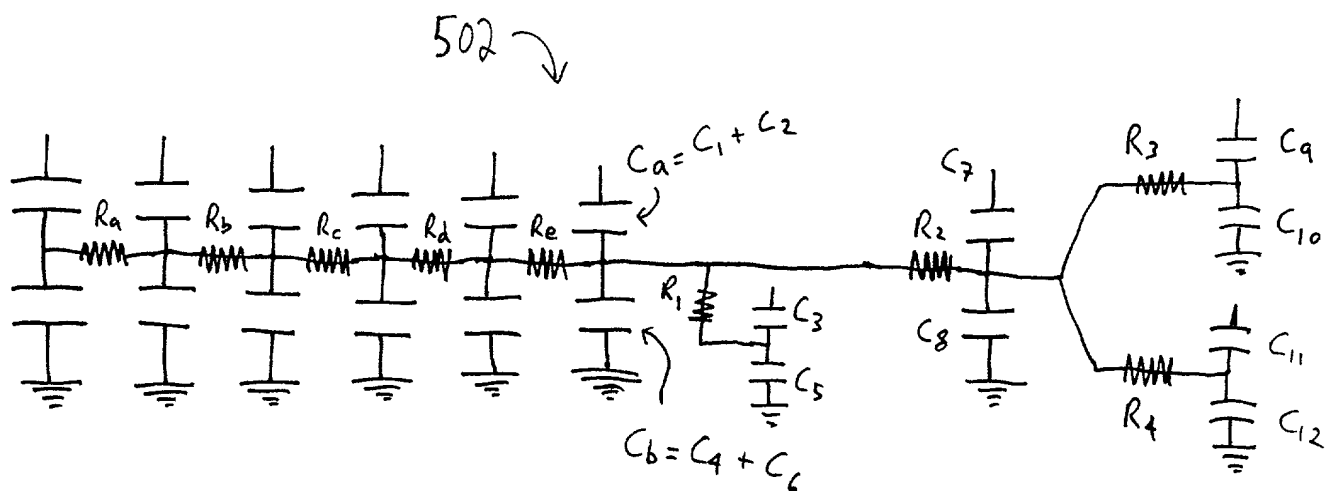


FIGURE 5B

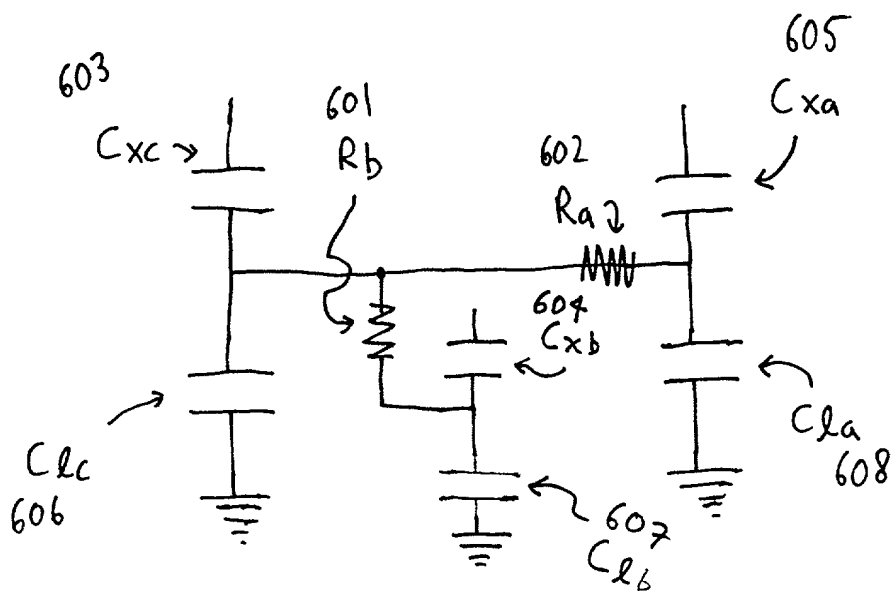


FIGURE 6A

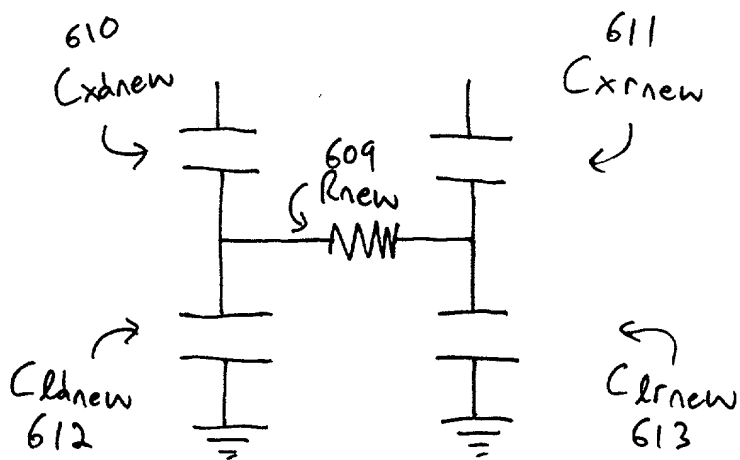


FIGURE 6B

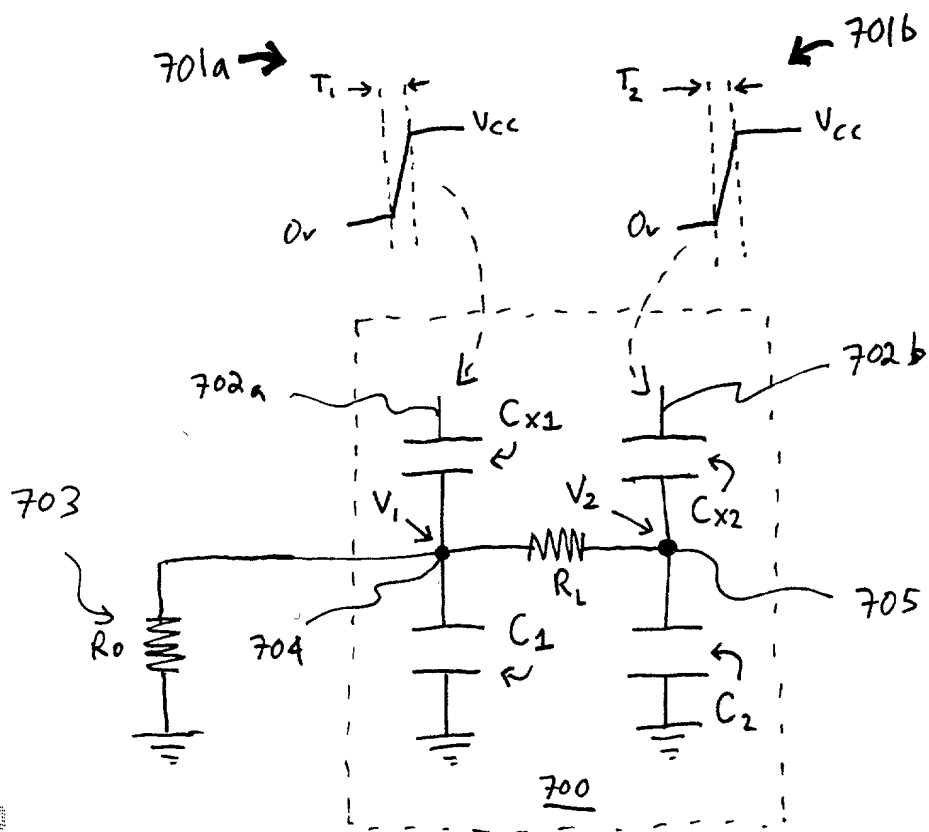


FIGURE 7a

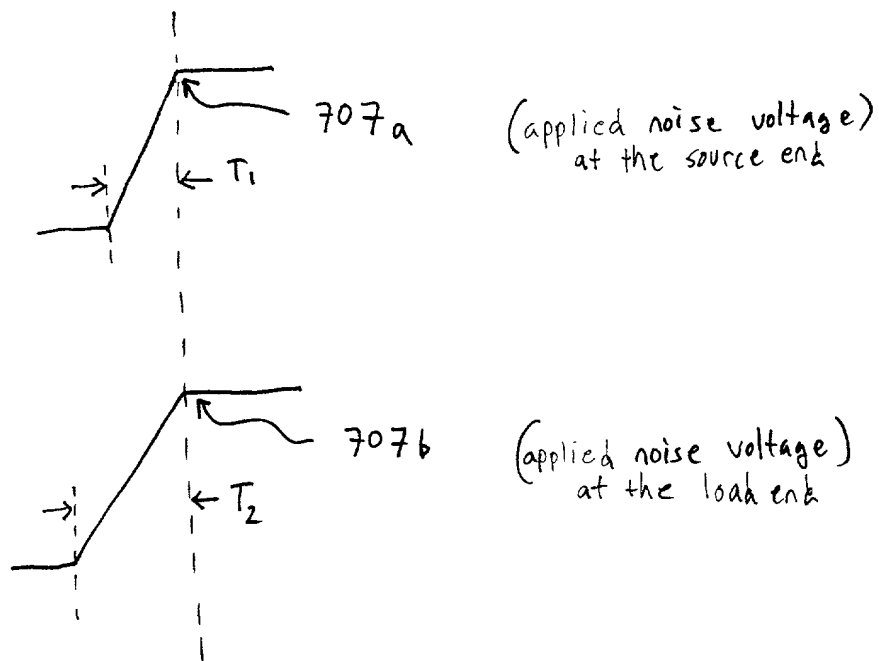


FIGURE 7b

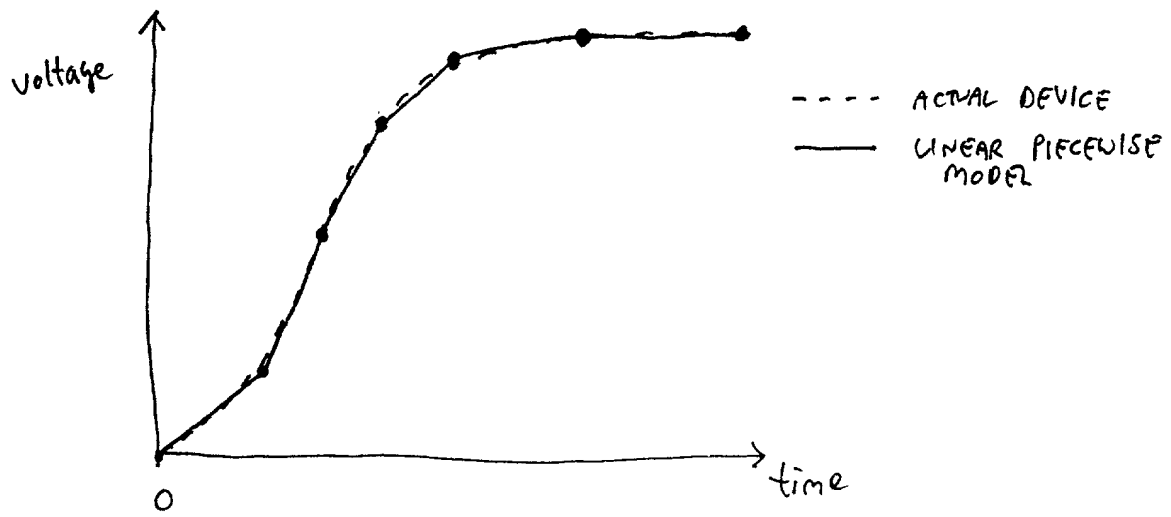


FIGURE 7C

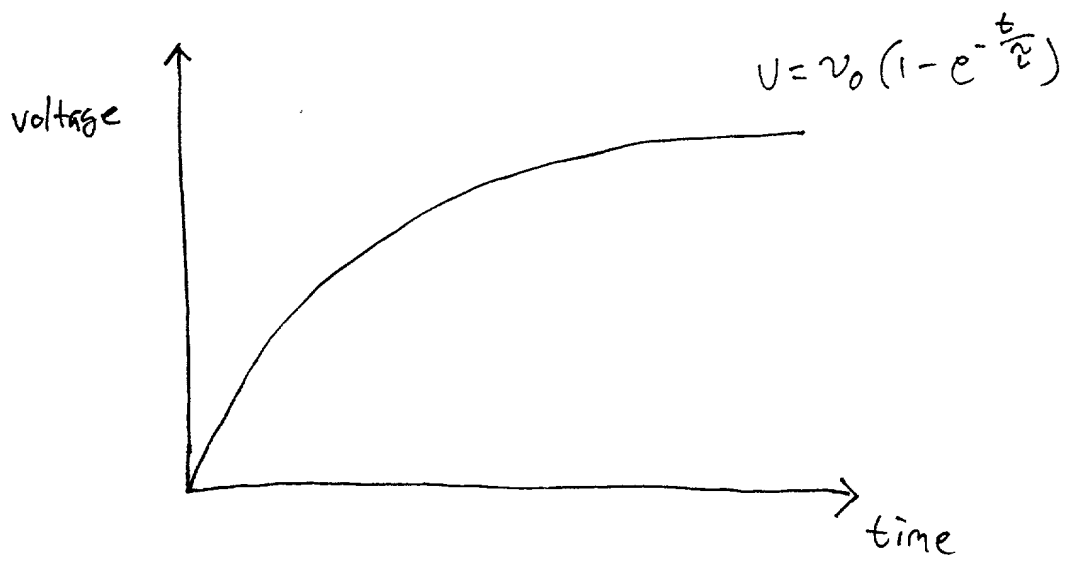


FIGURE 7D

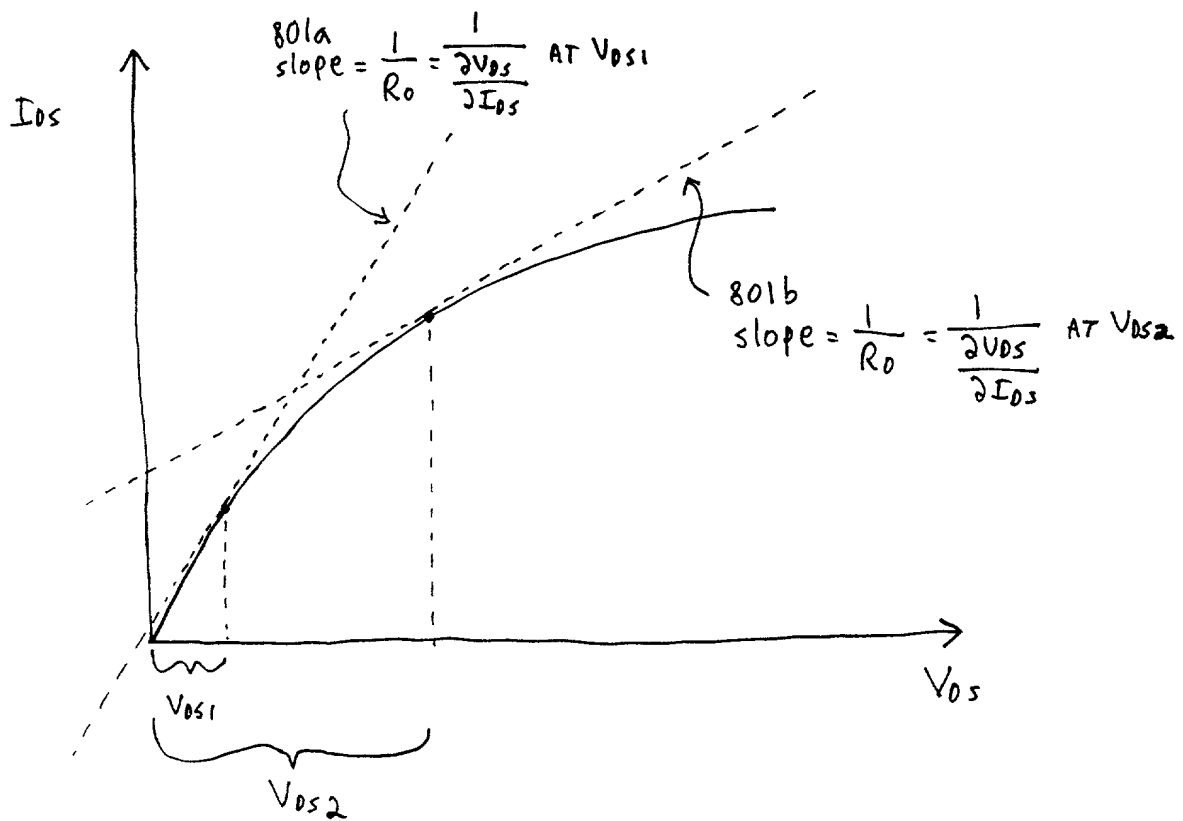


FIGURE 8A

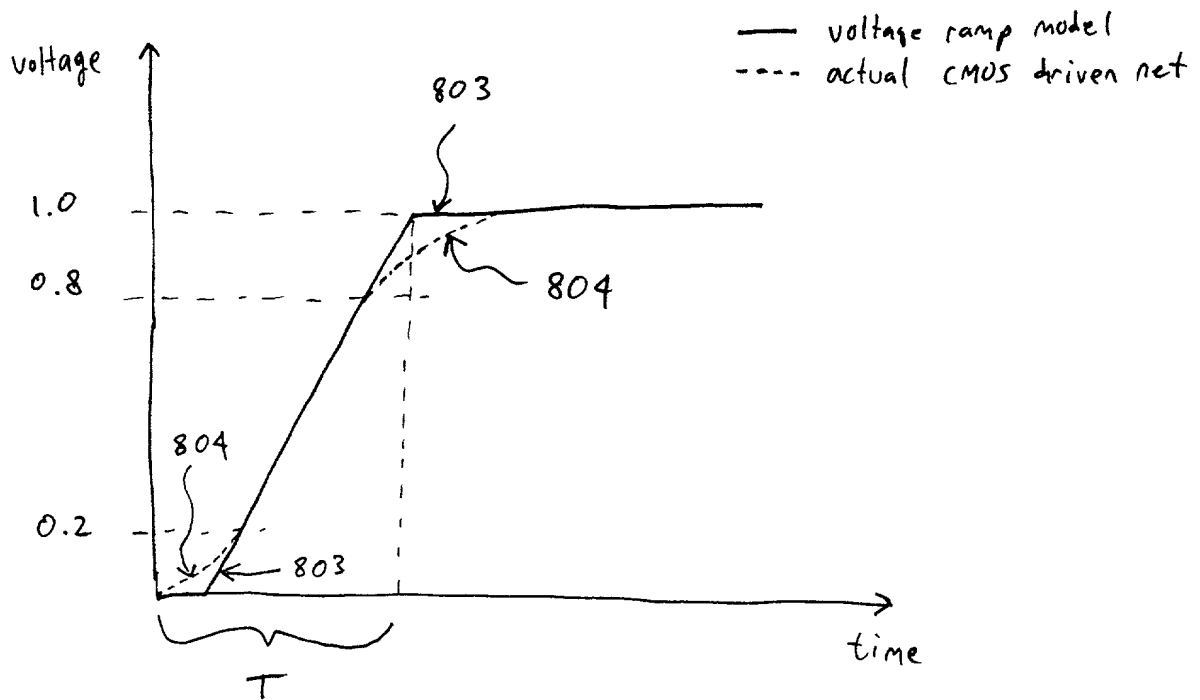


FIGURE 8B

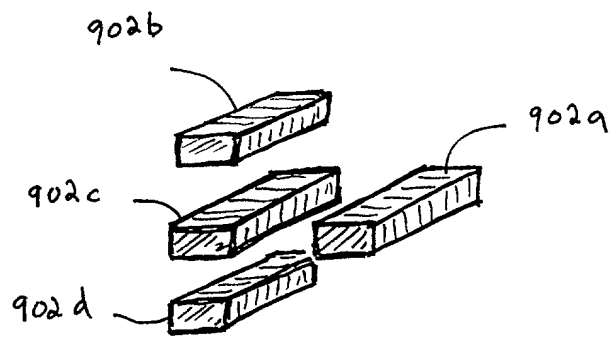


FIGURE 9A

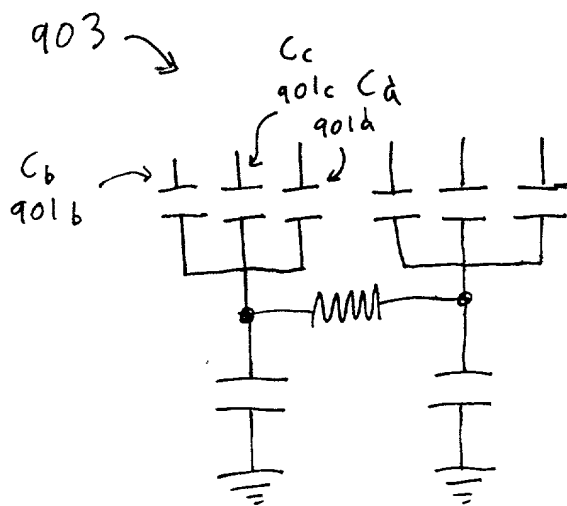


FIGURE 9B

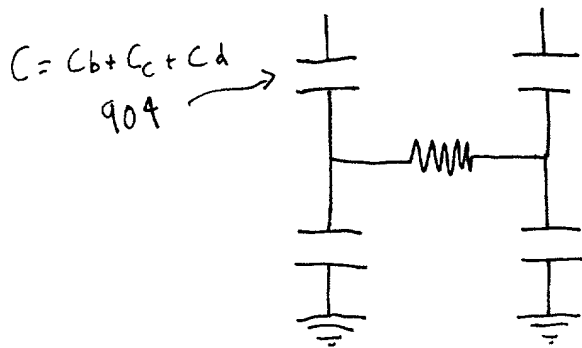
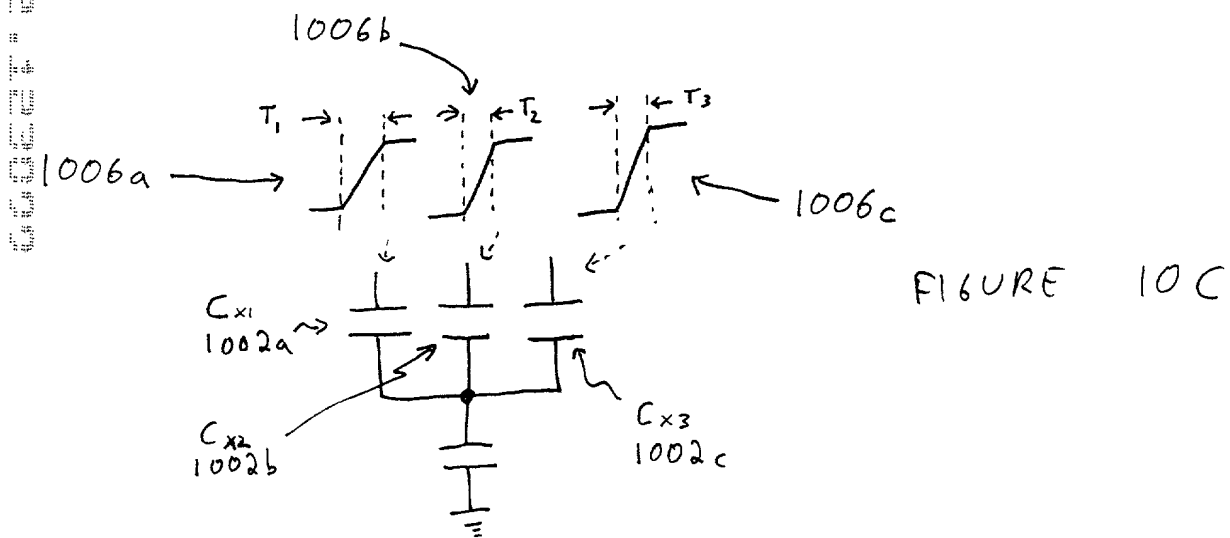
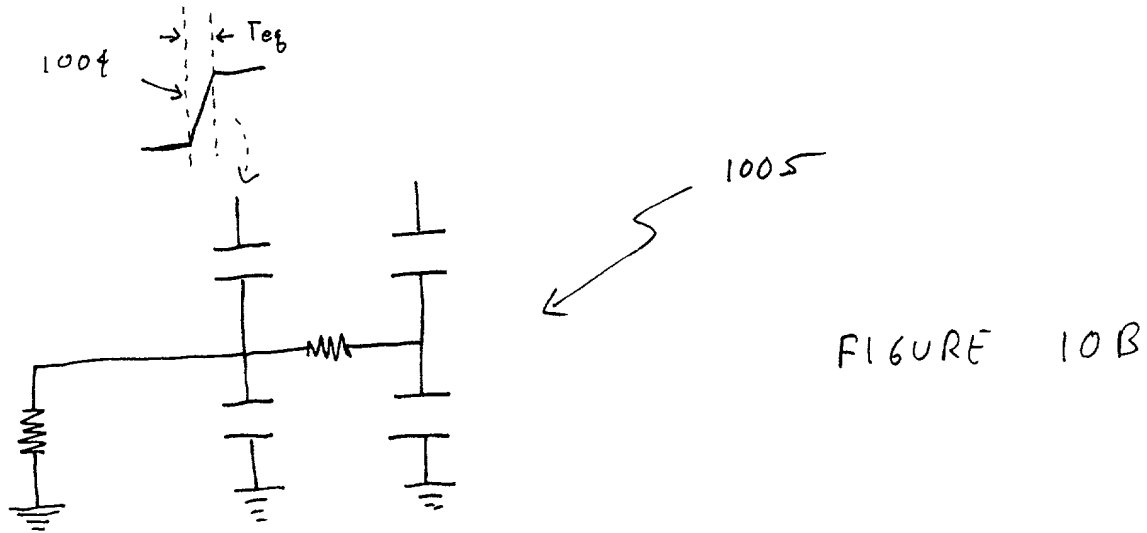
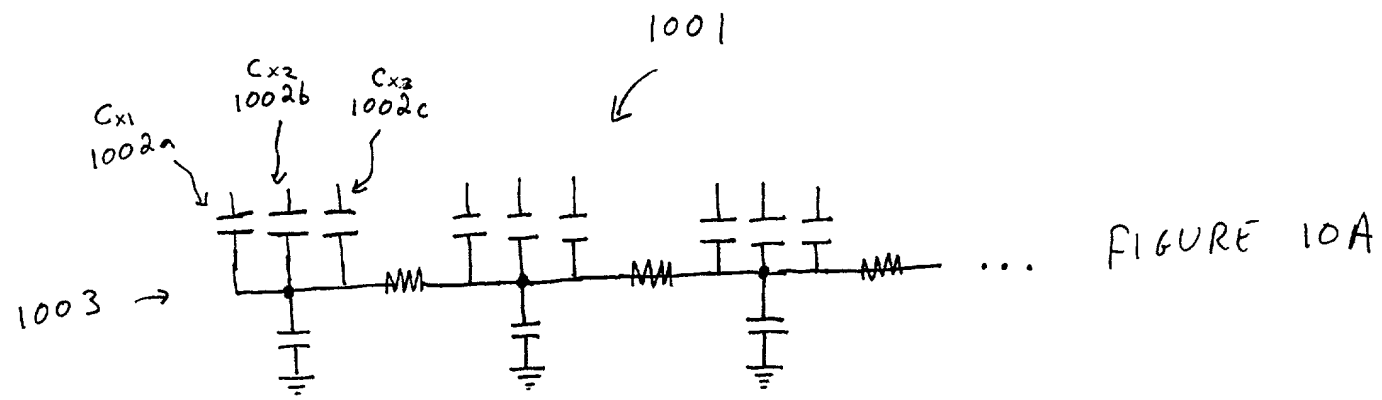


FIGURE 9C



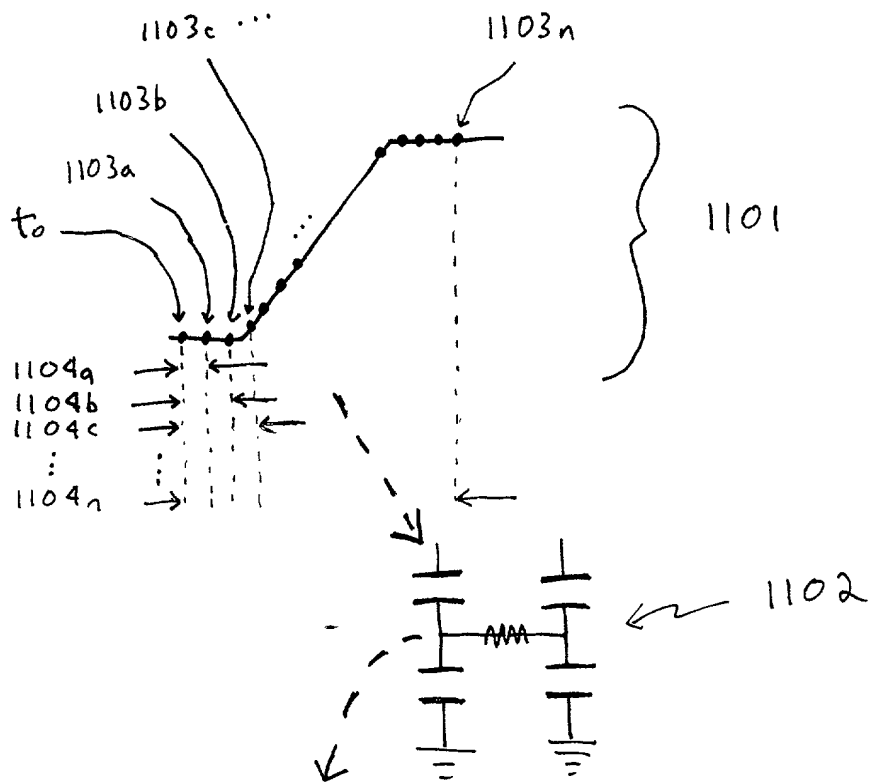


FIG. 11

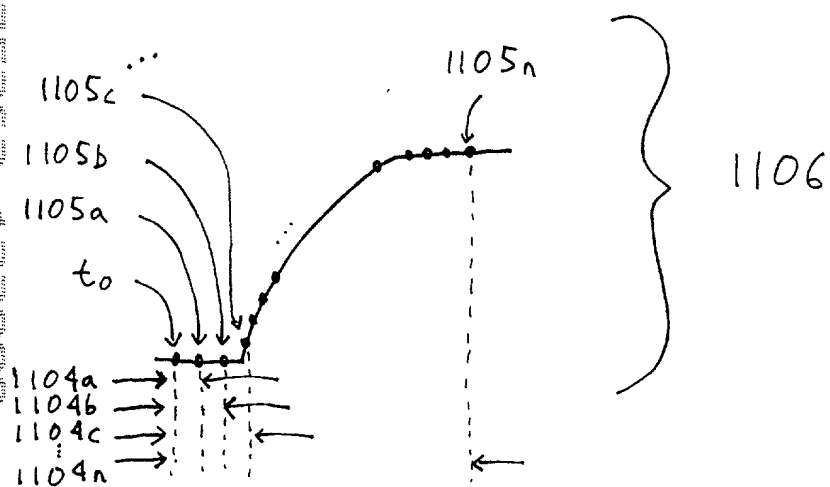


FIGURE 11

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Method and Apparatus for Calculating Interconnect Noise Due to Cross Capacitance in the Presence of Line Resistance

the specification of which

X is attached hereto.
_____ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

<u>Prior Foreign Application(s)</u>			<u>Priority Claimed</u>	
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	Yes	No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	Yes	No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

_____ Application Number	_____ Filing Date
_____ Application Number	_____ Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

_____ Application Number	_____ Filing Date	_____ Status -- patented, pending, abandoned
_____ Application Number	_____ Filing Date	_____ Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Darren J. Milliken, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct
telephone calls to Darren J. Milliken, (408) 720-8598.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Ben D. Roberts

Inventor's Signature  Date Dec 23, 1999

Residence Sunnyvale, California Citizenship USA
(City, State) (Country)

Post Office Address 1386 Bedford Avenue
Sunnyvale, California 94087

Full Name of Second/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____

Full Name of Third/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____

APPENDIX A

William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Ronald C. Card, Reg. No. P44,587; Thomas M. Coester, Reg. No. 39,637; Stephen M. De Klerk, under 37 C.F.R. § 10.9(b); Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. P41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W. Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Erica W. Kuo, Reg. No. 42,775; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. No. 42,004; Lisa A. Norris, Reg. No. P44,976; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Kimberley G. Nobles, Reg. No. 38,255; Daniel E. Ovanezian, Reg. No. 41,236; Babak Redjaian, Reg. No. 42,096; William F. Ryann, Reg. No. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey Sam Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; John F. Travis, Reg. No. 43,203; George G. C. Tseng, Reg. No. 41,355; Joseph A. Twarowski, Reg. No. 42,191; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Charles T. J. Weigell, Reg. No. 43,398; Kirk D. Williams, Reg. No. 42,229; James M. Wu, Reg. No. P45,241; Steven D. Yates, Reg. No. 42,242; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Andrew C. Chen, Reg. No. 43,544; Justin M. Dillon, Reg. No. 42,486; Paramita Ghosh, Reg. No. 42,806; and Sang Hui Kim, Reg. No. 40,450; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg. No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells; Reg. No. P43,256, Peter Lam, Reg. No. P44,855; and Gene I. Su, Reg. No. 45,140; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56 Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

- (1) Prior art cited in search reports of a foreign patent office in a counterpart application, and
 - (2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.
- (b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and
- (1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
 - (2) It refutes, or is inconsistent with, a position the applicant takes in:
 - (i) Opposing an argument of unpatentability relied on by the Office, or
 - (ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

- (1) Each inventor named in the application;
 - (2) Each attorney or agent who prepares or prosecutes the application; and
 - (3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.
- (d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.